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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/909,013 | 07/19/2001 | Makoto Yoshino | TIJ-29448 | 8724 |

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| EXAMINER | |
|---|---|
| GEYER, SCOTT B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2829 | |

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/909,013 | YOSHINO ET AL. | |
| | Examiner | Art Unit | |
| | Scott B. Geyer | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,13 and 16* is/are allowed.

6)☒ Claim(s) *5-10,12,14,15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

**1.** The rejections of claims 8, 9, 10 and 12 under 35 USC 112 (second paragraph) are withdrawn in light of the amendments to these claims by the applicant.

### *Claim Rejections - 35 USC § 102*

**2.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

**3.** Claims 5-10 and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Cho (6,235,555 B1).

**3A.** As to ***claim 5***, Cho teaches a method of forming an insulation film 68 which is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other.

**3B.** As to ***claim 6***, Cho teach a sprocket holes and through holes spaced at regular intervals, which thus have pitches **L** and **p**. As neither **n**, **m**, **L** or **p** are defined in the claim, two integers **n** and **m**, where **n<m**, could satisfy the equation **(m*p)=(n*L)**.

**3C.** As to ***claim 7***, Cho teach sprocket holes 71 formed along both sides of the insulation film 68. The sprocket holes are used to advance the film along, in combination with toothed sprocket mechanism. As the film is advanced, through holes are formed in the film (column 4, line 22 et seq.). Neither **n** nor **L** are defined by applicant's claim - - the sprockets taught by Cho have a pitch **L** and they are moved a length **n*L** by the sprocket tooth mechanism.

**3D.** As to ***claim 8***, Cho teaches a two dimensional conductor pattern (as evidenced by the conductor wires as seen in figure 9). Cho also teaches a conductive plating connected with the conductor pattern (column 5, lines 1-7).

**3E.** As to ***claim 9***, Cho teaches a method of forming an insulation film 68 which is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Cho also teaches a chip mounted to the insulation film and electrically connected to the conductive patterns of the insulation film, encapsulation of the mounted chip and separation of the insulation film into individual packages (see figure 13, numerals 92-95).

**3F.** As to ***claim 10***, Cho teaches plating of gold upon a layer of copper to make the conductive patterns (column 4, lines 66-67, continued to column 5, lines 1-7).

**3G.** As to ***claim 12***, Cho teaches a two dimensional conductor pattern (as evidenced by the conductor wires as seen in figure 9). Cho also teaches a conductive plating connected with the conductor pattern (column 5, lines 1-7).

### *Claim Rejections - 35 USC § 103*

**4.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5.** Claims 14, 15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (6,235,555 B1) in view of Hayashi et al. (6,192,579 B1).

**5A.** As to ***claim 14***, Cho teaches a method of packaging a semiconductor device, wherein an insulation film 68 is a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Cho also teaches mounting a semiconductor chip on the insulation film, encapsulating the chip in sealing resin and separating the film into individual resin coated chip packages (see

column 6, lines 33-49). Cho does not teach mounting a chip directly *over* the through holes. However, Hayashi et al. teach mounting a chip on an insulation film directly over through holes in the film, as shown by figures 5 and 8. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of Cho with the mounting method of Hayashi et al. so as to reduce the overall size of the individual package (i.e., reduce the footprint of the package).

**5B.** As to ***claim 15***, Cho teaches an insulation film 68 as a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Further, the through holes are arranged in relation to each other in an array and are formed continuously along and across the film and within the circuit regions.

**5C.** As to ***claim 17***, Cho teaches an insulation film 68 as a substrate for carrying a semiconductor chip 21, as seen in figure 9. The insulation film 68 has sprocket holes 71 formed at regular intervals along each side of the film, and thus have a pitch **L**. A two-dimensional array of through holes 62 are formed in insulation film 71 between the sprocket holes, and adjacent through holes are spaced at regular intervals from each other as is clearly shown in figure 10B, and thus have a pitch **p** in relation to each other. Further, the through holes are arranged in relation to each other in an array and are formed continuously along and across the film.

**5D.** As to ***claims 18 and 19***, Hayashi et al. teach formation of metal solder in the through holes (see column 6, lines 1-5).

### *Allowable Subject Matter*

**6.** Claims 11, 13 and 16 are allowed.

**7.** The following is a statement of reasons for the indication of allowable subject matter: Claims 11, 13 and 16 have been amended by the applicant to independent form, and contain allowable subject matter as indicated in the previous office action.

### *Response to Arguments*

**8.** Applicant's arguments filed June 22nd, 2004 have been fully considered. The applicant has argued on page 9 (of 10) that Cho teaches a *circuit board 70 as described on column 4, lines 35-40*, and that *a circuit board is not an insulation film*. While the examiner appreciates the distinction pointed out by the applicant, the examiner does not find this argument persuasive. Cho teaches in column 4, lines 22 et seq. that the *circuit board 70* as pointed out by the applicant is actually a "reel-deployed printed circuit board 70". As further taught by Cho, in column 3, lines 11 et seq., the reel-deployed printed circuit board material is comprised of a flexible base board glass-epoxy material, which is an insulating film material. Therefore, the base structure of the *circuit board 70* is an insulating glass-epoxy film material. Therefore, the process steps performed on the *circuit board 70* as taught by Cho may also be viewed as process steps performed on an insulting film, since the *circuit board 70* of Cho is merely an *insulting film* with

some circuitry on it. The fact that Cho's insulating film has metal circuitry on it does not exclude it as a valid reference against the applicant's instant claims, as applied in the above rejections.

***Conclusion***

**9. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**10.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT GEYER
PATENT EXAMINER

SBG
July 13, 2004

DAVID ZARNEKE
PRIMARY EXAMINER
7/12/04